Architecture overview

Sergeev Efim
Senior software engineer
Singularis Lab, Ltd.
Intel® Many Integrated Core (Intel MIC) Architecture

Targeted at highly parallel HPC workloads
- Physics, Chemistry, Biology, Financial Services

Power efficient cores, support for parallelism
- Cores: less speculation, threads, wider SIMD
- Scalability: high BW on die interconnect and memory

General Purpose Programming Environment
- Runs Linux (full service, open source OS)
- Runs applications written in Fortran, C, C++, ...
- Supports X86 memory model, IEEE 754
- x86 collateral (libraries, compilers, Intel® VTune™ debuggers, etc)
Knights Corner Coprocessor

- Intel® Xeon® Processor
- PCIe x16
- System Memory
- TCP/IP

KNC Card
- > 50 Cores
- Linux OS
- >= 8GB GDDR5 memory

GDDR5 Channel

GDDR5 Channel
Intel® Xeon Phi™ Coprocessor Becomes a network Node

Intel® Xeon® Processor

Intel® Xeon Phi™ Coprocessor

Virtual Network Connection

Intel® Xeon® Processor

Intel® Xeon Phi™ Coprocessor

Virtual Network Connection

Intel® Xeon Phi™ Architecture + Linux enables IP addressability
• Getting full performance from the Intel® MIC architecture requires both a high degree of **parallelism** and **vectorization**
  – Not all code can be written this way
  – Not all programs make sense on this architecture
• Intel® MIC is different from Xeon
  – It specializes in running highly parallel and vectorized code.
  – Not optimized for processing serial code
• Parallelism and vectorization optimizations are beneficial across both architectures
Intel® Many Integrated Core (Intel MIC) Architecture

- 8 memory controllers
- 16 Channel GDDR5 MC
- PCIe GEN2

- Cores: 61 cores, at 1.1 GHz in-order, support 4 threads
- 512 bit Vector Processing Unit
- 32 native registers

- High-speed bi-directional ring interconnect
- Fully Coherent L2 Cache

- Reliability Features
  - Parity on L1 Cache, ECC on memory
  - CRC on memory IO, CAP on memory IO
Core Architecture Overview

60+ in-order, low power IA cores in a ring interconnect

Two pipelines
• Scalar Unit based on Pentium® processors
• Dual issue with scalar instructions
• Pipelined one-per-clock scalar throughput

SIMD Vector Processing Engine

4 hardware threads per core
• 4 clock latency, hidden by round-robin scheduling of threads
• two threads per core to achieve full compute potential

Coherent 512KB L2 Cache per core
Vector Instruction Performance

X86 specific logic < 2% of core + L2 area
Vector Processing Unit Extends Scalar IA Core

VPU contains 16 SP ALUs, 8 DP ALUs,

Most VPU instructions have a latency of 4 cycles and TPT 1 cycle
  • Load/Store/Scatter have 7-cycle latency
  • Convert/Shuffle have 6-cycle latency

VPU instructions are issued in u-pipe

Certain instructions can go to v-pipe also
  • Vector Mask, Vector Store, Vector Packstore, Vector Prefetch, Scalar
The Interconnect
Distributed Tag Directories

Tag Directories track cache-lines in all L2s
Interleaved Memory Access
Interconnect: 2X AD/AK
Benchmark: Theoretical maximum
(Intel® Xeon® processor E5-2670 vs. Intel® Xeon Phi™ coprocessor 5110P & SE10P/X)

Single Precision (GF/s)

<table>
<thead>
<tr>
<th></th>
<th>E5-2670 (2x 2.6GHz, 8C, 115W)</th>
<th>5110P (60C, 1.05GHz, 225W)</th>
<th>SE10P/X (61C, 1.1GHz, 300W)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Up to 3.2x</strong></td>
<td>666</td>
<td>2,022</td>
<td>2,147</td>
</tr>
<tr>
<td>Higher is Better</td>
<td></td>
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</table>

Double Precision (GF/s)

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</tr>
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<tbody>
<tr>
<td><strong>Up to 3.2x</strong></td>
<td>333</td>
<td>1,011</td>
<td>1,074</td>
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<tr>
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Memory Bandwidth (GB/s)

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<tr>
<th></th>
<th>E5-2670 (2x 2.6GHz, 8C, 115W)</th>
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<tbody>
<tr>
<td><strong>Up to 3.45x</strong></td>
<td>102</td>
<td>320</td>
<td>352</td>
</tr>
<tr>
<td>Higher is Better</td>
<td></td>
<td></td>
<td></td>
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Source: Intel as of October 17, 2012
Configuration Details: Please reference slide speaker notes.
For more information go to [http://www.intel.com/performance](http://www.intel.com/performance)
Benchmark: Synthetic Performance Summary

SGEMM (GF/s)

- Up to 2.9X
- Higher is Better

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<th>Baseline</th>
<th>5110P</th>
<th>SE10P</th>
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</thead>
<tbody>
<tr>
<td>640</td>
<td>1,729</td>
<td>1,860</td>
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</tbody>
</table>

| ES-2670 Baseline (2x 2.6GHz, 8C, 115W) | 5110P (60C, 1.053GHz, 225W) | SE10P (61C, 1.1GHz, 300W) |

DGEMM (GF/s)

- Up to 2.8X
- Higher is Better

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<tr>
<th>Baseline</th>
<th>5110P</th>
<th>SE10P</th>
</tr>
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<tbody>
<tr>
<td>309</td>
<td>833</td>
<td>883</td>
</tr>
</tbody>
</table>

| ES-2670 Baseline (2x 2.67GHz, 8C, 115W) | 5110P (60C, 1.053GHz, 225W) | SE10P (61C, 1.1GHz, 300W) |

SMP Linpack (GF/s)

- Up to 2.6X
- Higher is Better

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<tr>
<td>303</td>
<td>722</td>
<td>803</td>
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| ES-2670 Baseline (2x 2.7GHz, 8C, 115W) | 5110P (60C, 1.053GHz, 225W) | SE10P (61C, 1.1GHz, 300W) |

Coprocessor results: Benchmark run 100% on coprocessor, no help from Intel® Xeon® processor host (aka native)
Thank you!

Sergeev Efim

- efim.sergeev@singularis-lab.com

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